

form *pnp* transistors compared with fabricating *nnp* transistors. The base width of 50 nm for an *nnp* and 30 nm for a *pnp* were achieved simultaneously by low-energy ion implantation and rapid thermal annealing for emitter drive in. Cutoff frequencies of 30 and 32, and current gain of 120 and 80 were obtained in *nnp* and *pnp* transistors, respectively, in the same chip. Simulated results show that the power dissipation is reduced to 1/5 in a complementary active pull-down circuit compared to the conventional ECL circuit.

It is difficult, however, to achieve same cutoff frequency and the Early voltage because the excess upward diffusion of boron from the buried layer in *pnp* transistor. A lower temperature process is necessary to completely suppress the upward diffusion to obtain the higher Early voltage.

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#### REFERENCES

- [1] H. Itoh, T. Saitoh, T. Yamada, M. Yamamoto, and A. Masaki, "Advanced ECL with new active pull-down emitter followers," in *Proc. BCTM*, pp. 23-25, 1988.
- [2] K.-Y. Toh, C. T. Chuang, T. C. Chen, J. Warnock, G. P. Li, K. Chin, and T. Ning, "A 23 psec/2.1 mW ECL gate," in *ISSCC Dig. Tech. Papers*, pp. 224-225, 1989.
- [3] H. J. Shin, P.-F. Lu and C. T. Chuang, "A high-speed low-power JFET pull-down ECL circuit," in *Proc. BCTM*, pp. 136-139, 1990.
- [4] C. T. Chuang, K. Chin, P.-F. Lu, and H. J. Shin, "High-speed low-power Darlington ECL circuit," in *Dig. Tech. Papers Symp. VLSI Circuit*, pp. 80-81, 1992.
- [5] C. T. Chuang and D. D. Tang, "High-speed low-power ac-coupled complementary push-pull ECL circuit," *IEEE J. Solid-State Circuits*, vol. 27, pp. 660-663, 1992.
- [6] Y. Idei, N. Homma, T. Onai, K. Washio, T. Nishida, H. Nambu, and K. Kanetani, "Capacitor-coupled complementary emitter-follower for ultra-high-speed low-power bipolar logic circuit," in *Dig. Tech. Papers 1993 Symp. VLSI Circuits*, pp. 25-26, 1993.
- [7] H. J. Shin, "Self-feedback-controlled pull-down emitter follower for high-speed low-power bipolar logic circuits," in *Dig. Tech. Papers 1993 Symp. VLSI Circuits*, pp. 27-28, 1993.
- [8] T. Kuroda, T. Fujita, M. Noda, P. Thai, L. Yang, and D. Gray, "Capacitor-free level-sensitive active pull-down ECL circuit with self-adjusting driving capability," in *Dig. Tech. Papers 1993 Symp. VLSI Circuits*, pp. 29-30, 1993.
- [9] Y. Kobayashi, C. Yamaguchi, Y. Amemiya, and T. Sakai, "High performance LSI process technology: SST-CBi-CMOS," in *IEDM Tech. Dig.*, pp. 760-763, 1988.
- [10] J. Warnock, P.-F. Lu, T.-C. Chen, K. Y. Toh, J. D. Cressler, K. A. Jenkins, D. D. Tang, J. Burghartz, J. Y. C. Sun, C. T. Chuang, G. P. Li, and T. H. Ning, "A 27 GHz 20 psec pnp technology," in *IEDM Tech. Dig. Papers*, pp. 903-905, 1988.
- [11] J. Warnock, P.-F. Lu, J. D. Cressler, K. A. Jenkins, and J. Y. Sun, "35 GHz/36 psec ECL pnp technology," in *IEDM Tech. Dig. Papers*, pp. 301-304, 1990.
- [12] J. Warnock, J. D. Cressler, K. A. Jenkins, T. C. Chen, J. Y. Sun, and D. D. Tang, "50-GHz self-aligned silicon bipolar transistor with ion-implanted base profiles," *IEEE Electron Device Lett.*, 11, pp. 475-477, 1991.
- [13] K. Washio, H. Shimamoto and T. Nakamura, "A 35-GHz  $20 \mu\text{m}^2$  Self-aligned PNP technology for ultra-high-speed high-density complementary bipolar ULSI's," in *Dig. Tech. Papers 1992 Symp. VLSI Technol.*, pp. 64-65, 1992.
- [14] J. Warnock, J. D. Cressler, J. Burghartz, D. Harame, K. Jenkins, and C. T. Chuang, "High performance complementary bipolar technology," in *1993 Symp. VLSI Technol.*, pp. 75-76, 1993.
- [15] T. Onai, E. Ohue, Y. Idei, M. Tanabe, H. Shimamoto, K. Washio, and T. Nakamura, "An NPN 30 GHz, PNP 32 GHz,  $f_T$  complementary bipolar technology," in *IEDM Tech. Dig. Papers*, pp. 63-66, 1993.
- [16] T. Nakamura, T. Onai, N. Homma, T. Shiba, and Y. Tamaki, "Ultra-small high-speed bipolar transistor with sidewall silicide technology," in *Proc. BCTM*, pp. 11-16, 1991.
- [17] T. Shiba, Y. Tamaki, T. Onai, M. Saitoh, T. Kure, F. Murai, and T. Nakamura, "SPOTEC—A sub  $10 \mu\text{m}^2$  bipolar transistor structure using fully self-aligned sidewall polycide base technology," in *IEDM Tech. Dig.*, pp. 455-45, 1991.

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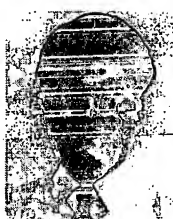
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